

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRX encoded:
				5 *
				6 * E705 VLREP - Vector Load and Replicate
				7 *
				8 * James Wekel March 2025
				9 *****
				11 *****
				12 *
				13 * basic instruction tests
				14 *
				15 *****
				16 * This program tests proper functioning of the z/arch E7 VRX
				17 * Vector Load and Replicate instruction.
				18 * Exceptions are not tested.
				19 *
				20 * NOTE: As VLREP is missing, this test uses the Extended Mnemonics:
				21 * VREPLB, VREPLH, VLREPF, VLREPG
				22 *
				23 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				24 * obvious coding errors. None of the tests are thorough. They are
				25 * NOT designed to test all aspects of any of the instructions.
				26 *
				27 *****
				28 *
				29 * *Testcase zvector-e7-23-VLREP
				30 * *
				31 * * Zvector E7 instruction tests for VRX encoded:
				32 * *
				33 * * E705 VLREP - Vector Load and Replicate
				34 * *
				35 * * # -----
				36 * * # This tests only the basic function of the instructions.
				37 * * # Exceptions are NOT tested.
				38 * * # -----
				39 * *
				40 * main size 2
				41 * numcpu 1
				42 * sysclear
				43 * archlvl z/Arch
				44 * *
				45 * loadcore "\$(testpath)/zvector-e7-23-VLREP.core" 0x0
				46 * *
				47 * diag8cmd enable # (needed for messages to Hercules console)
				48 * runtest 5
				49 * diag8cmd disable # (reset back to default)
				50 * *
				51 * *Done
				52 *
				53 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				55 *****
				56 * FCHECK Macro - Is a Facility Bit set?
				57 *
				58 * If the facility bit is NOT set, an message is issued and
				59 * the test is skipped.
				60 *
				61 * Fcheck uses R0, R1 and R2
				62 *
				63 * eg. FCHECK 134, 'vector-packed-decimal'
				64 *****
				65 MACRO
				66 FCHECK &BITNO, &NOTSETMSG
				67 . * &BITNO : facility bit number to check
				68 . * &NOTSETMSG : 'facility name'
				69 LCLA &FBBYTE Facility bit in Byte
				70 LCLA &FBBIT Facility bit within Byte
				71
				72 LCLA &L(8)
				73 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				74
				75 &FBBYTE SETA &BITNO/8
				76 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				77 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				78
				79 B X&SYSNDX
				80 * Fcheck data area
				81 * skip messgae
				82 SKT&SYSNDX DC C' Skipping tests: '
				83 DC C&NOTSETMSG
				84 DC C' (bit &BITNO) is not installed.'
				85 SKL&SYSNDX EQU *-SKT&SYSNDX
				86 * facility bits
				87 DS FD gap
				88 FB&SYSNDX DS 4FD
				89 DS FD gap
				90 *
				91 X&SYSNDX EQU *
				92 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				93 STFLE FB&SYSNDX get facility bits
				94
				95 XGR R0, R0
				96 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				97 N R0, =F' &FBBIT' is bit set?
				98 BNZ XC&SYSNDX
				99 *
				100 * facility bit not set, issue message and exit
				101 *
				102 LA R0, SKL&SYSNDX message length
				103 LA R1, SKT&SYSNDX message address
				104 BAL R2, MSG
				105
				106 B EOJ
				107 XC&SYSNDX EQU *
				108 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				110	*****
				111	* Low core PSWs
				112	*****
00000000		00000000	000016FB	113	ZVE7TST START 0
		00000000		114	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	115	
				116	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	118	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			119	DC X' 0000000180000000'
000001A8	00000000 00000200			120	DC AD(BEGIN)
000001B0		000001B0	000001D0	122	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			123	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			124	DC AD(X' DEAD')
000001E0		000001E0	00000200	126	ORG ZVE7TST+X' 200' Start of actual test program..
				128	*****
				129	* The actual "ZVE7TST" program itself...
				130	*****
				131	*
				132	* Architecture Mode: z/Arch
				133	* Register Usage:
				134	*
				135	* R0 (work)
				136	* R1- 4 (work)
				137	* R5 Testing control table - current test base
				138	* R6- R7 (work)
				139	* R8 First base register
				140	* R9 Second base register
				141	* R10 Third base register
				142	* R11 E7TEST call return
				143	* R12 E7TESTS register
				144	* R13 (work)
				145	* R14 Subroutine call
				146	* R15 Secondary Subroutine call or work
				147	*
				148	*****
00000200		00000200		150	USING BEGIN, R8 FIRST Base Register
00000200		00001200		151	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		152	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			154	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			155	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			156	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	158	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	159	LA R9, 2048(, R9) Inititalize SECOND base register
				160	

LOC	OBJECT CODE			ADDR1	ADDR2	STMT				
						256	*****			
						257	*	RPTERROR	Report instruction test in error	
						258	*****			
0000032C	50F0	8190			00000390	260	RPTERROR	ST	R15, RPTSAVE	Save return address
00000330	5050	8194			00000394	261		ST	R5, RPTSVR5	Save R5
						262	*			
00000334	4820	5004			00000004	263		LH	R2, TNUM	get test number and convert
00000338	4E20	8E73			00001073	264		CVD	R2, DECNUM	
0000033C	D211	8E5D	8E47	0000105D	00001047	265		MVC	PRT3, EDIT	
00000342	DE11	8E5D	8E73	0000105D	00001073	266		ED	PRT3, DECNUM	
00000348	D202	8E18	8E6A	00001018	0000106A	267		MVC	PRTNUM(3), PRT3+13	fill in message with test #
						268				
0000034E	D207	8E33	5008	00001033	00000008	269		MVC	PRTNAME, OPNAME	fill in message with instruction
						270	*			
00000354	E320	5007	0076		00000007	271		LB	R2, m3	get m3 and convert
0000035A	4E20	8E73			00001073	272		CVD	R2, DECNUM	
0000035E	D211	8E5D	8E47	0000105D	00001047	273		MVC	PRT3, EDIT	
00000364	DE11	8E5D	8E73	0000105D	00001073	274		ED	PRT3, DECNUM	
0000036A	D201	8E44	8E6B	00001044	0000106B	275		MVC	PRTm3(2), PRT3+14	fill in message with m3 field
						277	*			
						278	*	Use Hercules Diagnose for Message to console		
						279	*			
00000370	9002	8198			00000398	280		STM	R0, R2, RPTDWSAV	save regs used by MSG
00000374	4100	003F			0000003F	281		LA	R0, PRTLNG	message length
00000378	4110	8E08			00001008	282		LA	R1, PRTLNE	messagfe address
0000037C	4520	81A8			000003A8	283		BAL	R2, MSG	call Hercules console MSG display
00000380	9802	8198			00000398	284		LM	R0, R2, RPTDWSAV	restore regs
00000384	5850	8194			00000394	286		L	R5, RPTSVR5	Restore R5
00000388	58F0	8190			00000390	287		L	R15, RPTSAVE	Restore return address
0000038C	07FF					288		BR	R15	Return to caller
00000390	00000000					290	RPTSAVE	DC	F' 0'	R15 save area
00000394	00000000					291	RPTSVR5	DC	F' 0'	R5 save area
00000398	00000000	00000000				293	RPTDWSAV	DC	2D' 0'	R0- R2 save area for MSG call

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				411	*****
				412	* E7TEST DSECT
				413	*****
				415	E7TEST DSECT ,
00000000	00000000			416	TSUB DC A(0) pointer to test
00000004	0000			417	TNUM DC H' 00' Test Number
00000006	00			418	DC X' 00'
00000007	00			419	M3 DC HL1' 00' m3 used
				420	
00000008	40404040	40404040		421	OPNAME DC CL8' ' E7 name
00000010	00000000			422	V2ADDR DC A(0) address of v2 source
00000014	00000000			423	V3ADDR DC A(0) address of v3 source
00000018	00000000			424	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			425	READDR DC A(0) result (expected) address
00000020	00000000	00000000		426	DS FD gap
00000028	00000000	00000000		427	V10OUTPUT DS XL16 V1 Output
00000038	00000000	00000000		428	DS FD gap
				429	
				430	* test routine will be here (from VRX macro)
				431	*
				432	* followed by
				433	* EXPECTED RESULT
				435	ZVE7TST CSECT ,
000010B4		00000000	000016FB	436	DS 0F
				438	*****
				439	* Macros to help build test tables
				440	*****
				442	*
				443	* macro to generate individual test
				444	*
				445	MACRO
				446	VRX &INST, &M3
				447	. * &INST - VRX instruction under test
				448	. * &m3 - m3 field
				449	
				450	GBLA &TNUM
				451	&TNUM SETA &TNUM+1
				452	
				453	DS 0FD
				454	USING *, R5 base for test data and test routine
				455	
				456	T&TNUM DC A(X&TNUM) address of test routine
				457	DC H' &TNUM test number
				458	DC X' 00'
				459	DC HL1' &M3' m3
				460	DC CL8' &INST' instruction name
				461	DC A(RE&TNUM+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				506 *****	
				507 * E7 VRX tests	
				508 *****	
				509 PRINT DATA	
				510	
				511 * E705 VLREP - Vector Load and Replicate	
				512 *	
				513 * VRX instruction, m3	
				514 * followed by	
				515 * 16 byte expected result (V1)	
				516 * 16 byte source	
				517 *	
				518 *-----	
				519 * VLREP - Vector Load and Replicate	
				520 *-----	
				521 *Byte	
				522 VRX VLREPB, 0	
000010B8				523+ DS OFD	
000010B8		000010B8		524+ USING *, R5	base for test data and test routine
000010B8	000010F8			525+T1 DC A(X1)	address of test routine
000010BC	0001			526+ DC H' 1'	test number
000010BE	00			527+ DC X' 00'	
000010BF	00			528+ DC HL1' 0'	m3
000010C0	E5D3D9C5 D7C24040			529+ DC CL8' VLREPB'	instruction name
000010C8	00001124			530+ DC A(RE1+16)	address of v2 source
000010CC	00001134			531+ DC A(RE1+32)	address of v3 source
000010D0	00000010			532+ DC A(16)	result length
000010D4	00001114			533+REA1 DC A(RE1)	result address
000010D8	00000000 00000000			534+ DS FD	gap
000010E0	00000000 00000000			535+V101 DS XL16	V1 output
000010E8	00000000 00000000				
000010F0	00000000 00000000			536+ DS FD	gap
				537+*	
000010F8				538+X1 DS 0F	
000010F8	E760 8E94 0806	00001094		539+ VL v22, V1FUDGE	fudge v22
000010FE	E310 5010 0014	00000010		540+ LGF R1, V2ADDR	load source address
00001104	E760 1000 0805	00000000		541+ VLREPB V22, 0(0, R1)	test instruction
0000110A	E760 5028 080E	000010E0		542+ VST V22, V101	save v1 output
00001110	07FB			543+ BR R11	return
00001114				544+RE1 DC 0F	xl16 expected result
00001114				545+ DROP R5	
00001114	FFFFFFFF FFFFFFFF			546 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
0000111C	FFFFFFFF FFFFFFFF				
00001124	FFFFFFFF FFFFFFFF			547 DC XL16' FFFFFFFFFFFFFFFFFF 0102030405060708'	source
0000112C	01020304 05060708				
				548	
				549 VRX VLREPB, 0	
00001138				550+ DS OFD	
00001138		00001138		551+ USING *, R5	base for test data and test routine
00001138	00001178			552+T2 DC A(X2)	address of test routine
0000113C	0002			553+ DC H' 2'	test number
0000113E	00			554+ DC X' 00'	
0000113F	00			555+ DC HL1' 0'	m3
00001140	E5D3D9C5 D7C24040			556+ DC CL8' VLREPB'	instruction name
00001148	000011A4			557+ DC A(RE2+16)	address of v2 source
0000114C	000011B4			558+ DC A(RE2+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001150	00000010			559+	DC	A(16)	result length
00001154	00001194			560+REA2	DC	A(RE2)	result address
00001158	00000000 00000000			561+	DS	FD	gap
00001160	00000000 00000000			562+V102	DS	XL16	V1 output
00001168	00000000 00000000						
00001170	00000000 00000000			563+	DS	FD	gap
				564+*			
00001178				565+X2	DS	OF	
00001178	E760 8E94 0806		00001094	566+	VL	v22, V1FUDGE	fudge v22
0000117E	E310 5010 0014		00000010	567+	LGF	R1, V2ADDR	load source address
00001184	E760 1000 0805		00000000	568+	VLREPB	V22, 0(0, R1)	test instruction
0000118A	E760 5028 080E		00001160	569+	VST	V22, V102	save v1 output
00001190	07FB			570+	BR	R11	return
00001194				571+RE2	DC	OF	xl16 expected result
00001194				572+	DROP	R5	
00001194	01010101 01010101			573	DC	XL16' 0101010101010101 0101010101010101'	result t
0000119C	01010101 01010101						
000011A4	01020304 05060708			574	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	source
000011AC	090A0B0C 0D0E0F00						
				575			
000011B8				576	VRX	VLREPB, 0	
000011B8		000011B8		577+	DS	OFD	
000011B8	000011F8			578+	USING	*, R5	base for test data and test routine
000011BC	0003			579+T3	DC	A(X3)	address of test routine
000011BE	00			580+	DC	H' 3'	test number
000011BF	00			581+	DC	X' 00'	
000011C0	E5D3D9C5 D7C24040			582+	DC	HL1' 0'	m3
000011C8	00001224			583+	DC	CL8' VLREPB'	instruction name
000011CC	00001234			584+	DC	A(RE3+16)	address of v2 source
000011D0	00000010			585+	DC	A(RE3+32)	address of v3 source
000011D4	00001214			586+	DC	A(16)	result length
000011D8	00000000 00000000			587+REA3	DC	A(RE3)	result address
000011E0	00000000 00000000			588+	DS	FD	gap
000011E8	00000000 00000000			589+V103	DS	XL16	V1 output
000011F0	00000000 00000000			590+	DS	FD	gap
				591+*			
000011F8				592+X3	DS	OF	
000011F8	E760 8E94 0806		00001094	593+	VL	v22, V1FUDGE	fudge v22
000011FE	E310 5010 0014		00000010	594+	LGF	R1, V2ADDR	load source address
00001204	E760 1000 0805		00000000	595+	VLREPB	V22, 0(0, R1)	test instruction
0000120A	E760 5028 080E		000011E0	596+	VST	V22, V103	save v1 output
00001210	07FB			597+	BR	R11	return
00001214				598+RE3	DC	OF	xl16 expected result
00001214				599+	DROP	R5	
00001214	FEFEFEFE FEFEFEFE			600	DC	XL16' FEFEFEFEFEFEFEFE FEFEFEFEFEFEFEFE'	result t
0000121C	FEFEFEFE FEFEFEFE						
00001224	FEFDFCFB FAF9F8F7			601	DC	XL16' FEFDFCFBFAF9F8F7 090A0B0C0D0E0F00'	source
0000122C	090A0B0C 0D0E0F00						
				602			
				603 *Halfword			
00001238				604	VRX	VLREPH, 1	
00001238		00001238		605+	DS	OFD	
00001238	00001278			606+	USING	*, R5	base for test data and test routine
0000123C	0004			607+T4	DC	A(X4)	address of test routine
				608+	DC	H' 4'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000123E	00			609+	DC	X' 00'	
0000123F	01			610+	DC	HL1' 1'	m3
00001240	E5D3D9C5 D7C84040			611+	DC	CL8' VLREPH'	instruction name
00001248	000012A4			612+	DC	A(RE4+16)	address of v2 source
0000124C	000012B4			613+	DC	A(RE4+32)	address of v3 source
00001250	00000010			614+	DC	A(16)	result length
00001254	00001294			615+REA4	DC	A(RE4)	result address
00001258	00000000 00000000			616+	DS	FD	gap
00001260	00000000 00000000			617+V104	DS	XL16	V1 output
00001268	00000000 00000000						
00001270	00000000 00000000			618+	DS	FD	gap
				619+*			
00001278				620+X4	DS	0F	
00001278	E760 8E94 0806		00001094	621+	VL	v22, V1FUDGE	fudge v22
0000127E	E310 5010 0014		00000010	622+	LGF	R1, V2ADDR	load source address
00001284	E760 1000 1805		00000000	623+	VLREPH	V22, 0(0, R1)	test instruction
0000128A	E760 5028 080E		00001260	624+	VST	V22, V104	save v1 output
00001290	07FB			625+	BR	R11	return
00001294				626+RE4	DC	0F	xl16 expected result
00001294				627+	DROP	R5	
00001294	FFAAFFAA FFAAFFAA			628	DC	XL16' FFAAFFAAFFAAFFAA FFAAFFAAFFAAFFAA'	result t
0000129C	FFAAFFAA FFAAFFAA						
000012A4	FFAAFFFF FFFFFFFF			629	DC	XL16' FFAAFFFFFFFFFFFFFFF 0102030405060708'	source
000012AC	01020304 05060708						
				630			
				631	VRX	VLREPH, 1	
000012B8				632+	DS	0FD	
000012B8		000012B8		633+	USING	*, R5	base for test data and test routine
000012B8	000012F8			634+T5	DC	A(X5)	address of test routine
000012BC	0005			635+	DC	H' 5'	test number
000012BE	00			636+	DC	X' 00'	
000012BF	01			637+	DC	HL1' 1'	m3
000012C0	E5D3D9C5 D7C84040			638+	DC	CL8' VLREPH'	instruction name
000012C8	00001324			639+	DC	A(RE5+16)	address of v2 source
000012CC	00001334			640+	DC	A(RE5+32)	address of v3 source
000012D0	00000010			641+	DC	A(16)	result length
000012D4	00001314			642+REA5	DC	A(RE5)	result address
000012D8	00000000 00000000			643+	DS	FD	gap
000012E0	00000000 00000000			644+V105	DS	XL16	V1 output
000012E8	00000000 00000000						
000012F0	00000000 00000000			645+	DS	FD	gap
				646+*			
000012F8				647+X5	DS	0F	
000012F8	E760 8E94 0806		00001094	648+	VL	v22, V1FUDGE	fudge v22
000012FE	E310 5010 0014		00000010	649+	LGF	R1, V2ADDR	load source address
00001304	E760 1000 1805		00000000	650+	VLREPH	V22, 0(0, R1)	test instruction
0000130A	E760 5028 080E		000012E0	651+	VST	V22, V105	save v1 output
00001310	07FB			652+	BR	R11	return
00001314				653+RE5	DC	0F	xl16 expected result
00001314				654+	DROP	R5	
00001314	01020102 01020102			655	DC	XL16' 0102010201020102 0102010201020102'	result t
0000131C	01020102 01020102						
00001324	01020304 05060708			656	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	source
0000132C	090A0B0C 0D0E0F00						
				657			
				658	VRX	VLREPH, 1	

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00001338				659+	DS	0FD	
00001338		00001338		660+	USING	*, R5	base for test data and test routine
00001338	00001378			661+T6	DC	A(X6)	address of test routine
0000133C	0006			662+	DC	H' 6'	test number
0000133E	00			663+	DC	X' 00'	
0000133F	01			664+	DC	HL1' 1'	m3
00001340	E5D3D9C5 D7C84040			665+	DC	CL8' VLREPH'	instruction name
00001348	000013A4			666+	DC	A(RE6+16)	address of v2 source
0000134C	000013B4			667+	DC	A(RE6+32)	address of v3 source
00001350	00000010			668+	DC	A(16)	result length
00001354	00001394			669+REA6	DC	A(RE6)	result address
00001358	00000000 00000000			670+	DS	FD	gap
00001360	00000000 00000000			671+V106	DS	XL16	V1 output
00001368	00000000 00000000						
00001370	00000000 00000000			672+	DS	FD	gap
				673+*			
00001378				674+X6	DS	0F	
00001378	E760 8E94 0806		00001094	675+	VL	v22, V1FUDGE	fudge v22
0000137E	E310 5010 0014		00000010	676+	LGF	R1, V2ADDR	load source address
00001384	E760 1000 1805		00000000	677+	VLREPH	V22, 0(0, R1)	test instruction
0000138A	E760 5028 080E		00001360	678+	VST	V22, V106	save v1 output
00001390	07FB			679+	BR	R11	return
00001394				680+RE6	DC	0F	xl16 expected result
00001394				681+	DROP	R5	
00001394	07FD07FD 07FD07FD			682	DC	XL16' 07FD07FD07FD07FD 07FD07FD07FD07FD'	result t
0000139C	07FD07FD 07FD07FD						
000013A4	07FD07FD 07FD07FD						
000013A4	07FD07FD 07FD07FD						
000013AC	07FD07FD 07FD07FD						
				683	DC	XL16' 07FD07FD07FD07FD 07FD07FD07FD07FD'	source
				684			
				685 *Word			
				686	VRX	VLREPF, 2	
000013B8				687+	DS	0FD	
000013B8		000013B8		688+	USING	*, R5	base for test data and test routine
000013B8	000013F8			689+T7	DC	A(X7)	address of test routine
000013BC	0007			690+	DC	H' 7'	test number
000013BE	00			691+	DC	X' 00'	
000013BF	02			692+	DC	HL1' 2'	m3
000013C0	E5D3D9C5 D7C64040			693+	DC	CL8' VLREPF'	instruction name
000013C8	00001424			694+	DC	A(RE7+16)	address of v2 source
000013CC	00001434			695+	DC	A(RE7+32)	address of v3 source
000013D0	00000010			696+	DC	A(16)	result length
000013D4	00001414			697+REA7	DC	A(RE7)	result address
000013D8	00000000 00000000			698+	DS	FD	gap
000013E0	00000000 00000000			699+V107	DS	XL16	V1 output
000013E8	00000000 00000000						
000013F0	00000000 00000000			700+	DS	FD	gap
				701+*			
000013F8				702+X7	DS	0F	
000013F8	E760 8E94 0806		00001094	703+	VL	v22, V1FUDGE	fudge v22
000013FE	E310 5010 0014		00000010	704+	LGF	R1, V2ADDR	load source address
00001404	E760 1000 2805		00000000	705+	VLREPF	V22, 0(0, R1)	test instruction
0000140A	E760 5028 080E		000013E0	706+	VST	V22, V107	save v1 output
00001410	07FB			707+	BR	R11	return
00001414				708+RE7	DC	0F	xl16 expected result
00001414				709+	DROP	R5	
00001414	01020304 01020304			710	DC	XL16' 0102030401020304 0102030401020304'	result t

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000141C	01020304 01020304						
00001424	01020304 05060708			711	DC	XL16' 0102030405060708 090A0B0C0D0E0F00'	source
0000142C	090A0B0C 0D0E0F00						
				712			
				713	VRX	VLREPF, 2	
00001438				714+	DS	OFD	
00001438		00001438		715+	USING	*, R5	base for test data and test routine
00001438	00001478			716+T8	DC	A(X8)	address of test routine
0000143C	0008			717+	DC	H' 8'	test number
0000143E	00			718+	DC	X' 00'	
0000143F	02			719+	DC	HL1' 2'	m3
00001440	E5D3D9C5 D7C64040			720+	DC	CL8' VLREPF'	instruction name
00001448	000014A4			721+	DC	A(RE8+16)	address of v2 source
0000144C	000014B4			722+	DC	A(RE8+32)	address of v3 source
00001450	00000010			723+	DC	A(16)	result length
00001454	00001494			724+REA8	DC	A(RE8)	result address
00001458	00000000 00000000			725+	DS	FD	gap
00001460	00000000 00000000			726+V108	DS	XL16	V1 output
00001468	00000000 00000000						
00001470	00000000 00000000			727+	DS	FD	gap
				728+*			
00001478				729+X8	DS	OF	
00001478	E760 8E94 0806		00001094	730+	VL	v22, V1FUDGE	fudge v22
0000147E	E310 5010 0014		00000010	731+	LGF	R1, V2ADDR	load source address
00001484	E760 1000 2805		00000000	732+	VLREPF	V22, 0(0, R1)	test instruction
0000148A	E760 5028 080E		00001460	733+	VST	V22, V108	save v1 output
00001490	07FB			734+	BR	R11	return
00001494				735+RE8	DC	OF	xl16 expected result
00001494				736+	DROP	R5	
00001494	F9F8F704 F9F8F704			737	DC	XL16' F9F8F704F9F8F704 F9F8F704F9F8F704'	result
0000149C	F9F8F704 F9F8F704						
000014A4	F9F8F704 05060708			738	DC	XL16' F9F8F70405060708 FFFFFFFFFFFFFFFFFF'	source
000014AC	FFFFFFFF FFFFFFFF						
				739			
				740	VRX	VLREPF, 2	
000014B8				741+	DS	OFD	
000014B8		000014B8		742+	USING	*, R5	base for test data and test routine
000014B8	000014F8			743+T9	DC	A(X9)	address of test routine
000014BC	0009			744+	DC	H' 9'	test number
000014BE	00			745+	DC	X' 00'	
000014BF	02			746+	DC	HL1' 2'	m3
000014C0	E5D3D9C5 D7C64040			747+	DC	CL8' VLREPF'	instruction name
000014C8	00001524			748+	DC	A(RE9+16)	address of v2 source
000014CC	00001534			749+	DC	A(RE9+32)	address of v3 source
000014D0	00000010			750+	DC	A(16)	result length
000014D4	00001514			751+REA9	DC	A(RE9)	result address
000014D8	00000000 00000000			752+	DS	FD	gap
000014E0	00000000 00000000			753+V109	DS	XL16	V1 output
000014E8	00000000 00000000						
000014F0	00000000 00000000			754+	DS	FD	gap
				755+*			
000014F8				756+X9	DS	OF	
000014F8	E760 8E94 0806		00001094	757+	VL	v22, V1FUDGE	fudge v22
000014FE	E310 5010 0014		00000010	758+	LGF	R1, V2ADDR	load source address
00001504	E760 1000 2805		00000000	759+	VLREPF	V22, 0(0, R1)	test instruction
0000150A	E760 5028 080E		000014E0	760+	VST	V22, V109	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001510	07FB			761+	BR	R11	return
00001514				762+RE9	DC	0F	xl16 expected result
00001514				763+	DROP	R5	
00001514	08080807 08080807			764	DC	XL16' 0808080708080807 0808080708080807'	result t
0000151C	08080807 08080807						
00001524	08080807 080807F7			765	DC	XL16' 08080807080807F7 FEFDFCFBFAF9F8F7'	source
0000152C	FEFDFCFB FAF9F8F7						
				766			
				767 *Doubleword			
				768	VRX	VLREPG, 3	
00001538				769+	DS	0FD	
00001538		00001538		770+	USING	*, R5	base for test data and test routine
00001538	00001578			771+T10	DC	A(X10)	address of test routine
0000153C	000A			772+	DC	H' 10'	test number
0000153E	00			773+	DC	X' 00'	
0000153F	03			774+	DC	HL1' 3'	m3
00001540	E5D3D9C5 D7C74040			775+	DC	CL8' VLREPG'	instruction name
00001548	000015A4			776+	DC	A(RE10+16)	address of v2 source
0000154C	000015B4			777+	DC	A(RE10+32)	address of v3 source
00001550	00000010			778+	DC	A(16)	result length
00001554	00001594			779+REA10	DC	A(RE10)	result address
00001558	00000000 00000000			780+	DS	FD	gap
00001560	00000000 00000000			781+V1010	DS	XL16	V1 output
00001568	00000000 00000000						
00001570	00000000 00000000			782+	DS	FD	gap
				783+*			
00001578				784+X10	DS	0F	
00001578	E760 8E94 0806		00001094	785+	VL	v22, V1FUDGE	fudge v22
0000157E	E310 5010 0014		00000010	786+	LGF	R1, V2ADDR	load source address
00001584	E760 1000 3805		00000000	787+	VLREPG	V22, 0(0, R1)	test instruction
0000158A	E760 5028 080E		00001560	788+	VST	V22, V1010	save v1 output
00001590	07FB			789+	BR	R11	return
00001594				790+RE10	DC	0F	xl16 expected result
00001594				791+	DROP	R5	
00001594	FFFFFFFF FFFF09AA			792	DC	XL16' FFFFFFFFFFFFFF09AA FFFFFFFFFFFFFF09AA'	result t
0000159C	FFFFFFFF FFFF09AA						
000015A4	FFFFFFFF FFFF09AA			793	DC	XL16' FFFFFFFFFFFFFF09AA 0102030405060708'	source
000015AC	01020304 05060708						
				794			
000015B8				795	VRX	VLREPG, 3	
000015B8		000015B8		796+	DS	0FD	
000015B8	000015F8			797+	USING	*, R5	base for test data and test routine
000015BC	000B			798+T11	DC	A(X11)	address of test routine
000015BE	00			799+	DC	H' 11'	test number
000015BF	03			800+	DC	X' 00'	
000015C0	E5D3D9C5 D7C74040			801+	DC	HL1' 3'	m3
000015C8	00001624			802+	DC	CL8' VLREPG'	instruction name
000015CC	00001634			803+	DC	A(RE11+16)	address of v2 source
000015D0	00000010			804+	DC	A(RE11+32)	address of v3 source
000015D4	00001614			805+	DC	A(16)	result length
000015D8	00000000 00000000			806+REA11	DC	A(RE11)	result address
000015E0	00000000 00000000			807+	DS	FD	gap
000015E8	00000000 00000000			808+V1011	DS	XL16	V1 output
000015F0	00000000 00000000			809+	DS	FD	gap
				810+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000015F8				811+X11	DS	0F		
000015F8	E760 8E94 0806		00001094	812+	VL	v22, V1FUDGE	fudge v22	
000015FE	E310 5010 0014		00000010	813+	LGF	R1, V2ADDR	load source address	
00001604	E760 1000 3805		00000000	814+	VLREPG	V22, 0(0, R1)	test instruction	
0000160A	E760 5028 080E		000015E0	815+	VST	V22, V1011	save v1 output	
00001610	07FB			816+	BR	R11	return	
00001614				817+RE11	DC	0F	xl16 expected result	
00001614				818+	DROP	R5		
00001614	AABB1122 05060708			819	DC	XL16' AABB112205060708 AABB112205060708'	result t	
0000161C	AABB1122 05060708							
00001624	AABB1122 05060708			820	DC	XL16' AABB112205060708 090A0B0C0D0E0F00'	source	
0000162C	090A0B0C 0D0E0F00							
				821				
				822	VRX	VLREPG, 3		
00001638				823+	DS	0FD		
00001638		00001638		824+	USING	*, R5	base for test data and test routine	
00001638	00001678			825+T12	DC	A(X12)	address of test routine	
0000163C	000C			826+	DC	H' 12'	test number	
0000163E	00			827+	DC	X' 00'		
0000163F	03			828+	DC	HL1' 3'	m3	
00001640	E5D3D9C5 D7C74040			829+	DC	CL8' VLREPG'	instruction name	
00001648	000016A4			830+	DC	A(RE12+16)	address of v2 source	
0000164C	000016B4			831+	DC	A(RE12+32)	address of v3 source	
00001650	00000010			832+	DC	A(16)	result length	
00001654	00001694			833+REA12	DC	A(RE12)	result address	
00001658	00000000 00000000			834+	DS	FD	gap	
00001660	00000000 00000000			835+V1012	DS	XL16	V1 output	
00001668	00000000 00000000							
00001670	00000000 00000000			836+	DS	FD	gap	
				837+*				
00001678				838+X12	DS	0F		
00001678	E760 8E94 0806		00001094	839+	VL	v22, V1FUDGE	fudge v22	
0000167E	E310 5010 0014		00000010	840+	LGF	R1, V2ADDR	load source address	
00001684	E760 1000 3805		00000000	841+	VLREPG	V22, 0(0, R1)	test instruction	
0000168A	E760 5028 080E		00001660	842+	VST	V22, V1012	save v1 output	
00001690	07FB			843+	BR	R11	return	
00001694				844+RE12	DC	0F	xl16 expected result	
00001694				845+	DROP	R5		
00001694	FEFDFCFB FAF9F801			846	DC	XL16' FEFDFCFBFAF9F801 FEFDFCFBFAF9F801'	result t	
0000169C	FEFDFCFB FAF9F801							
000016A4	FEFDFCFB FAF9F801			847	DC	XL16' FEFDFCFBFAF9F801 090A0B0C0D0E0F00'	source	
000016AC	090A0B0C 0D0E0F00							
				848				
				849				
000016B4	00000000			850	DC	F' 0'	END OF TABLE	
000016B8	00000000			851	DC	F' 0'		
				852 *				
				853 *	table of pointers to individual load test			
				854 *				
000016BC				855 E7TESTS	DS	0F		
				856	PTTABLE			
000016BC				857+TTABLE	DS	0F		
000016BC	000010B8			858+	DC	A(T1)		
000016C0	00001138			859+	DC	A(T2)		
000016C4	000011B8			860+	DC	A(T3)		
000016C8	00001238			861+	DC	A(T4)		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				877	*****
				878	* Register equates
				879	*****
		00000000	00000001	881 R0	EQU 0
		00000001	00000001	882 R1	EQU 1
		00000002	00000001	883 R2	EQU 2
		00000003	00000001	884 R3	EQU 3
		00000004	00000001	885 R4	EQU 4
		00000005	00000001	886 R5	EQU 5
		00000006	00000001	887 R6	EQU 6
		00000007	00000001	888 R7	EQU 7
		00000008	00000001	889 R8	EQU 8
		00000009	00000001	890 R9	EQU 9
		0000000A	00000001	891 R10	EQU 10
		0000000B	00000001	892 R11	EQU 11
		0000000C	00000001	893 R12	EQU 12
		0000000D	00000001	894 R13	EQU 13
		0000000E	00000001	895 R14	EQU 14
		0000000F	00000001	896 R15	EQU 15
				898	*****
				899	* Register equates
				900	*****
		00000000	00000001	902 V0	EQU 0
		00000001	00000001	903 V1	EQU 1
		00000002	00000001	904 V2	EQU 2
		00000003	00000001	905 V3	EQU 3
		00000004	00000001	906 V4	EQU 4
		00000005	00000001	907 V5	EQU 5
		00000006	00000001	908 V6	EQU 6
		00000007	00000001	909 V7	EQU 7
		00000008	00000001	910 V8	EQU 8
		00000009	00000001	911 V9	EQU 9
		0000000A	00000001	912 V10	EQU 10
		0000000B	00000001	913 V11	EQU 11
		0000000C	00000001	914 V12	EQU 12
		0000000D	00000001	915 V13	EQU 13
		0000000E	00000001	916 V14	EQU 14
		0000000F	00000001	917 V15	EQU 15
		00000010	00000001	918 V16	EQU 16
		00000011	00000001	919 V17	EQU 17
		00000012	00000001	920 V18	EQU 18
		00000013	00000001	921 V19	EQU 19
		00000014	00000001	922 V20	EQU 20
		00000015	00000001	923 V21	EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
R9	U	00000009	1	890	151	158	159	161	
RE1	F	00001114	4	544	530	531	533		
RE10	F	00001594	4	790	776	777	779		
RE11	F	00001614	4	817	803	804	806		
RE12	F	00001694	4	844	830	831	833		
RE2	F	00001194	4	571	557	558	560		
RE3	F	00001214	4	598	584	585	587		
RE4	F	00001294	4	626	612	613	615		
RE5	F	00001314	4	653	639	640	642		
RE6	F	00001394	4	680	666	667	669		
RE7	F	00001414	4	708	694	695	697		
RE8	F	00001494	4	735	721	722	724		
RE9	F	00001514	4	762	748	749	751		
REA1	A	000010D4	4	533					
REA10	A	00001554	4	779					
REA11	A	000015D4	4	806					
REA12	A	00001654	4	833					
REA2	A	00001154	4	560					
REA3	A	000011D4	4	587					
REA4	A	00001254	4	615					
REA5	A	000012D4	4	642					
REA6	A	00001354	4	669					
REA7	A	000013D4	4	697					
REA8	A	00001454	4	724					
REA9	A	000014D4	4	751					
READDR	A	0000001C	4	425	222				
REG2LOW	U	000000DD	1	368					
REG2PATT	U	AABBCCDD	1	367					
RELEN	A	00000018	4	424					
RPTDWSAV	D	00000398	8	293	280	284			
RPTERROR	I	0000032C	4	260	235				
RPTSAVE	F	00000390	4	290	260	287			
RPTSVR5	F	00000394	4	291	261	286			
SKL0001	U	0000004E	1	180	196				
SKT0001	C	0000022A	20	177	180	197			
SVOLDPSW	U	00000140	0	116					
T1	A	000010B8	4	525	858				
T10	A	00001538	4	771	867				
T11	A	000015B8	4	798	868				
T12	A	00001638	4	825	869				
T2	A	00001138	4	552	859				
T3	A	000011B8	4	579	860				
T4	A	00001238	4	607	861				
T5	A	000012B8	4	634	862				
T6	A	00001338	4	661	863				
T7	A	000013B8	4	689	864				
T8	A	00001438	4	716	865				
T9	A	000014B8	4	743	866				
TESTING	F	00001004	4	379	216				
TNUM	H	00000004	2	417	215	263			
TSUB	A	00000000	4	416	219				
TTABLE	F	000016BC	4	857					
V0	U	00000000	1	902					
V1	U	00000001	1	903	218				
V10	U	0000000A	1	912					
V11	U	0000000B	1	913					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X7	F	000013F8	4	702	689
X8	F	00001478	4	729	716
X9	F	000014F8	4	756	743
XC0001	U	000002D0	1	200	192
ZVE7TST	J	00000000	5884	113	116 118 122 126 377 114
=A(E7TESTS)	A	00000498	4	355	206
=AL2(L' MSGMSG)	R	000004A2	2	358	305
=F' 1'	F	0000049C	4	356	241
=F' 64'	F	00000494	4	354	191
=H' 0'	H	000004A0	2	357	300

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image Region CSECT	IMAGE	5884	0000-16FB	0000-16FB
		5884	0000-16FB	0000-16FB
	ZVE7TST	5884	0000-16FB	0000-16FB

STMT	FILE NAME
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100	100

```
1 /home/tn529/sharedvfp/tests/zvector-e7-23-VLREP.asm
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**** NO ERRORS FOUND ****